Gate Ref

(12) UK Patent Application (19) GB (11) 2 305 295 (13) A

(43) Date of A Publication 02.04.1997

(21) Application No 9619116.8

(22) Date of Filing 12.09.1996

(30) Priority Data
(31) 95030005 (32) 14.09.1995 (33) KR

(51) INT CL[6]
H01L 21/316

(52) UK CL (Edition O)
H1K KJAP K1CA K5B2 K5B3 K5B5 K5B9 K5C3G

(56) Documents Cited
EP 0249173 A1 US 5003062 A

(58) Field of Search
UK CL (Edition O) H1K KHAE KJAB KJACX KJAP KJAX
INT CL[6] H01L 21/314 21/316
Online:WPI

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(54) **Method for forming interlayer insulating film of semiconductor device**

(57) A method for forming an interlayer insulating film of a semiconductor device is capable of avoiding a field inversion phenomenon between the drain and source 113 of a parasitic MOSFET. The method includes the steps of preparing a semiconductor substrate 101 having an under-layer metal wiring 117 formed on an upper surface thereof, forming a barrier layer 121 on an exposed surface of the semiconductor substrate, coating a spin-on-glass film 123 over the barrier layer and then baking the spin-on-glass film, and forming an insulating film 125 over the spin-on-glass film. The device so formed also includes a second wiring layer 127, a BPSG film 115 and a protective nitride layer 129.

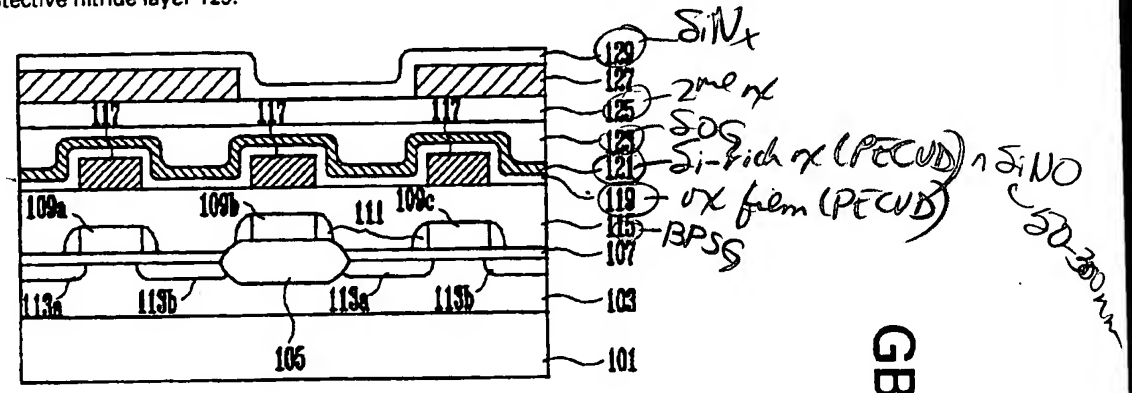


Fig . 2

GB 2 305 295 A

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

This print takes account of replacement documents submitted after the date of filing to enable the application to comply with the formal requirements of the Patents Rules 1995

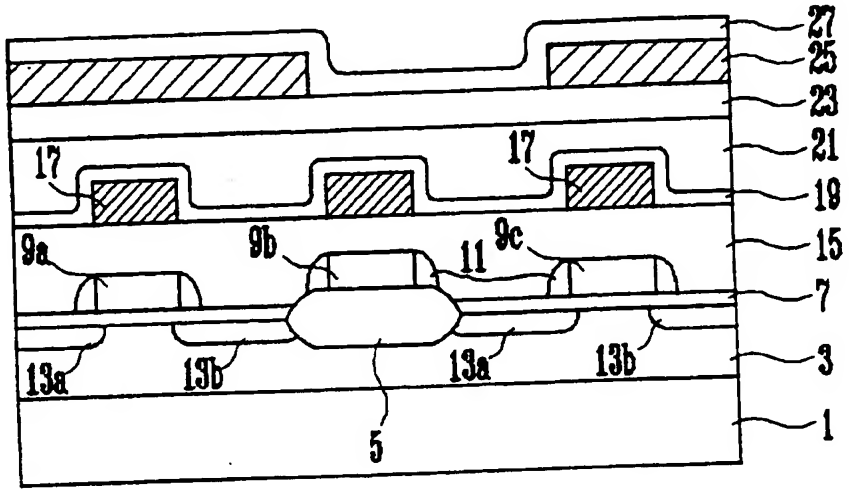


Fig . 1
Prior art

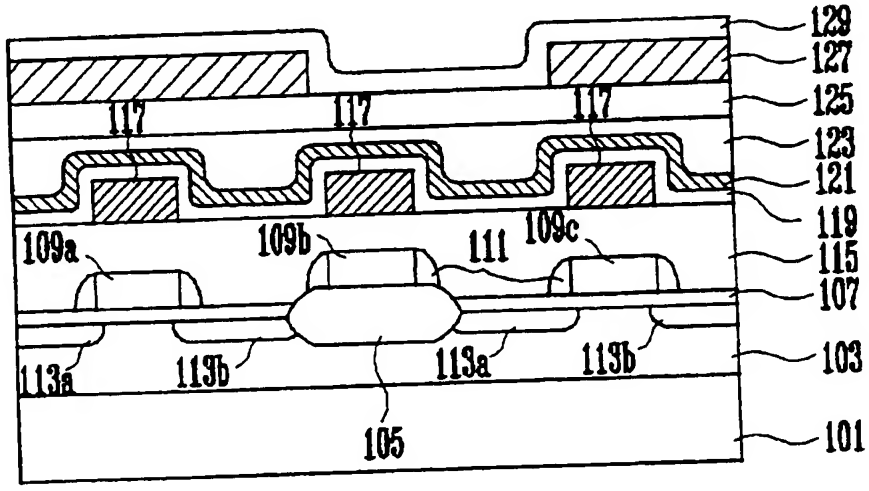


Fig . 2

Fig . 3

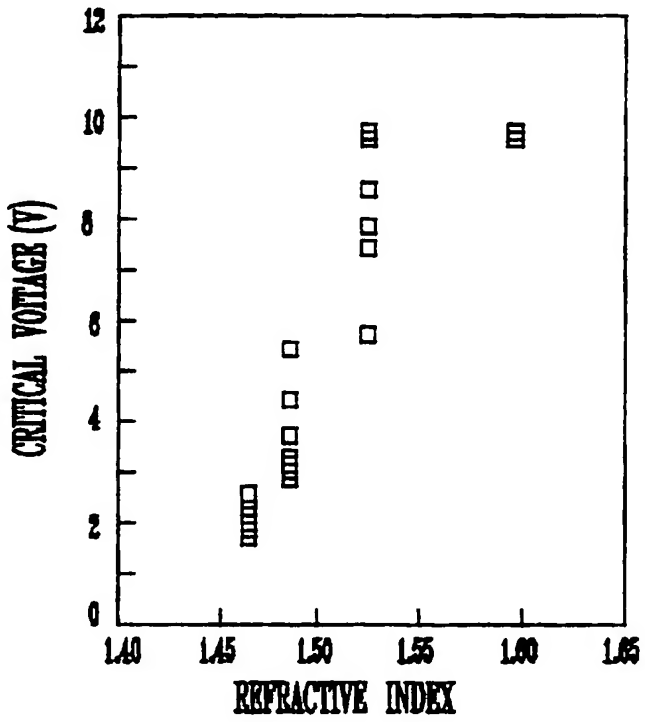
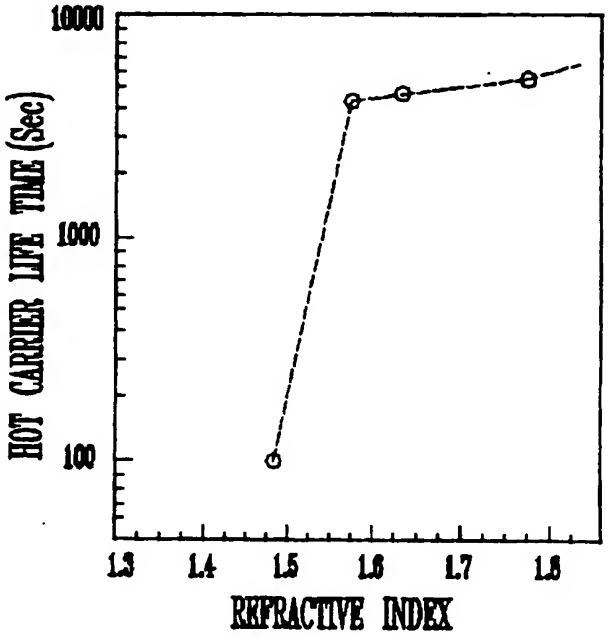

CRITICAL VOTAGE (V)
0
2
4
6
8
10
12
1.40
1.45
1.50
1.55
1.60
1.65
REFRACTIVE INDEX

Fig . 4


HOT CARRIER LIFE TIME (Sec)
10000
1000
100
1.3
1.4
1.5
1.6
1.7
1.8
REFRACTIVE INDEX

METHOD FOR FORMING INTERLAYER INSULATING FILM OF SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method for fabricating a semiconductor device, and more particularly to a method for forming an interlayer insulating film of a semiconductor device.

Description of the Prior Art

In the planarization of a CMOS device having a multilayer wiring structure, spin on glass (SOG) is typically used as an interlayer insulating film. A metal wiring is formed on the uppermost layer. A protective film made of SiN_x is deposited over the metal wiring.

Since H, OH, H_2O, etc. contained in the SOG film and SiN_x penetrate into the semiconductor device upon conducting a subsequent thermal process, a field inversion phenomenon may occur in that the insulation property between the drain and source of a parasitic MOSFET is degraded.

As a result, the threshold voltage between the drain and source is lowered whereas the leakage of current increases. For this reason, there is a problem in that the operation characteristic of the device becomes unstable.

In this connection, a conventional method for forming a CMOS device having a double-layer metal wiring structure will now be described in conjunction with FIG. 1.

FIG. 1 is a sectional view illustrating a semiconductor device having a double-layer wiring structure to which an interlayer insulating film formed in accordance with the prior art is applied.

In accordance with this method, a semiconductor substrate 1 is first prepared, and a P-type well 3 is then formed in the semiconductor substrate 1, as shown in FIG. 1. A field oxide film 5 is formed on the surface of the P-type well 3 to define active and field regions. A gate oxide film 7 is then formed over the active region of the P-type well 3. Gate electrodes (9a)(9b)(9c) are subsequently formed on the gate oxide film 7.

Thereafter, impurity ions are implanted in the semiconductor substrate 1 at both sides of each of the gate electrodes (9a)(9b)(9c), thereby forming source/drain regions 13. Thus, two normal MOSFET's respectively consisting of elements 9a, 13a and 13b and elements 9c, 13a and 13b, and a parasitic MOSFET consisting of elements 9b, 13a and 13b.

Subsequently, a boro-phosphor silicate glass (BPSG) film 15 is deposited over the entire upper surface of the resulting structure, thereby providing a planarized upper surface. A first-layer metal wiring 17 is then formed on a desired portion of the BPSG film 15.

Over the resulting structure, a first interlayer insulating film 19, a second interlayer insulating film 21 and a third interlayer insulating film 23 are then sequentially laminated in accordance with the plasma enhanced chemical vapor deposition (PECVD) method.

A second-layer metal wiring 25 is then formed on the third interlayer insulating film 23. SiN_x is then deposited over the second-layer metal wiring 25, thereby forming a surface protection film 27.

In the above-mentioned method for forming an interlayer insulating film, however, a field inversion phenomenon occurs between the drain and source of the n-channel parasitic MOSFET upon conducting a thermal processing after the deposition of the surface

protection film made of SiN_x. Such a field inversion phenomenon occurs as hydrogen contained in the protection film diffuses downwardly and reacts with OH, CH_3, H_2O, etc. contained in the SOG film, thereby producing a reaction product. This reaction product penetrates into the device through the interlayer insulating film.

The field inversion phenomenon also results from OH and H_2O contained in the SOG film. The OH and H_2O contained in the SOG film serve as a donor type impurity as they penetrate into the semiconductor device or generate positive charge in the field oxide film.

In other words, the reason why such a field inversion phenomenon occurs is because the under interlayer insulating film can not prevent the impurity produced upon conducting the process from penetrating into the device.

As a result, the threshold voltage between the drain and source is lowered, and the leakage of current increases. For this reason, a problem is created in that the operation characteristic of the device becomes unstable. This results in erroneous operation.

SUMMARY OF THE INVENTION

Therefore, an object of the invention is to provide a method for forming an interlayer insulating film of a semiconductor device, capable of avoiding a field inversion phenomenon between the drain and source of a parasitic MOSFET.

Another object of the invention is to provide a method for forming an interlayer insulating film of a semiconductor device, capable of achieving an improvement in the characteristic of the interlayer insulating film, thereby obtaining an improvement in the reliability of the semiconductor device.

Another object of the invention is to provide a method for forming an interlayer insulating film of a semiconductor device, capable of achieving the formation of an interlayer insulating film applicable to highly integrated semiconductor devices.

In accordance with one aspect of the present invention, a method for forming an interlayer insulating film of a semiconductor device comprises the steps of: providing a semiconductor substrate having a under-layer metal wiring formed on an upper surface thereof; forming a barrier layer on an exposed surface of the semiconductor substrate; coating a spin-on-glass film over the barrier layer and then baking the spin-on-glass film; and forming an insulating film over the spin-on-glass film.

In accordance with another aspect of the present invention, a method for forming an interlayer insulating film of a semiconductor device comprises the steps of: providing a semiconductor substrate having a under-layer metal wiring formed on an upper surface thereof; forming a silicon-rich oxide film over an exposed surface of the semiconductor substrate, forming a silicon nitride oxide film over the silicon-rich oxide film; forming a spin-on-glass film over the silicon nitride oxide film; and forming an oxide film over the spin-on-glass film.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and aspects of the invention will become apparent from the following description of embodiments with reference to the accompanying drawings in which:

FIG. 1 is a sectional view illustrating a semiconductor device having a double-layer wiring structure to which an interlayer insulating film formed in accordance with the prior art is applied;

FIG. 2 is a sectional view illustrating a semiconductor device having a double-layer metal wiring structure to which an interlayer insulating film formed in accordance with the present invention is

applied;

FIG. 3 is a graph depicting the relationship of the refractivity of the insulating film according to the present invention with the insulation-breaking critical voltage; and

FIG. 4 is a graph depicting the relationship between the refractivity of the insulating film and the life of hot carriers in each MOSFET.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 2 is a sectional view illustrating a semiconductor device having a double-layer metal wiring structure to which an interlayer insulating film formed in accordance with the present invention is applied.

In accordance with the present invention, a semiconductor substrate 101 is first prepared, and a P-type well 103 is then formed in a desired portion of the semiconductor substrate 101, as shown in FIG. 2. A field oxide film 105 is then formed on the surface of the P-type well 103 to define active and field regions.

A gate oxide film 107 is then formed over the active region of the P-type well 103. Gate electrodes 109a, 109b and 109c are subsequently formed on desired portions of the gate oxide film 7, respectively. The well 103 may have an N-type conductivity in accordance with the conductivity of the semiconductor substrate 101.

Thereafter, side wall spacers 111 are formed on opposite side surfaces of each gate electrode 109a, 109b or 109c. Using the gate electrodes 109a, 109b and 109c as a mask, impurity ions having a conductivity opposite to the P-type well 103 are implanted in the semiconductor substrate 101, thereby forming source regions 113a and drain regions 113b.

Thus, two normal MOSFET's respectively consisting of elements 109a,1 13a and 113b and elements 109b, 113a and 113b, and a parasitic MOSFET consisting of elements 109b, 113a and 113b.

Subsequently, a BPSG film 115 is deposited over the entire upper surface of the resulting structure, thereby providing a planarized upper surface. A first-layer metal wiring 117 is then formed on a desired portion of the BPSG film 115.

Over the entire upper surface of the resulting structure including the exposed surfaces of the BPSG film 115 and first-layer metal wiring 117, a first interlayer insulating film 119 and a silicon-rich oxide film 121 are then sequentially laminated in accordance with the PECVD method.

The silicon-rich oxide film 121 is deposited to a thickness from about 500 to 3,000Å. The first interlayer insulating film 119 is comprised of an oxide film and silicon-rich oxide film 121 which are used as an under interlayer insulating film.

As the semiconductor device has an increased integration degree, the interval between adjacent lines of the first-layer metal wiring is reduced to, for example, about 4 μm or less in DRAM devices of 256 Mega grade. Taking this fact into consideration, the under interlayer insulating film may consist of only the silicon-rich oxide film in accordance with another embodiment of the present invention, instead of both the first oxide film 119 and silicon-rich oxide film . This is because in the case of laminating both the first oxide film and silicon-rich oxide film, the space between adjacent lines of the metal wiring is too narrow to coat an SOG film thereon.

See also P8

The deposition of the silicon-rich oxide film 121 is carried out while increasing the flow rate of SiH_4 as a silicon source, but decreasing the flow rate of N_2O as an oxygen source in the

deposition of a silicon oxide film using the well-known PECVD method.

When the pressure ratio of SiH_4 to N_2O increases, the refractivity of the film increases to about 1.55 or more.

The stress state of the film can be controlled to correspond to a compressive stress state of -0.5 to -1.5 dyne/cm^2 by controlling radio frequency power.

Alternatively, the silicon-rich oxide film 121 may be deposited using a reactive gas of $SiH_4/N_4O/NH_3/N_2$ in accordance with the well-known PECVD method. In this case, the deposition of the silicon-rich oxide film 121 is carried out under the conditions in which the flow rate of SiH_4 is about 300 to 600 SCCM, the flow rate of N_2O is about 4,000 to 7,000 SCCM and the flow rate of N_2 is about 3,000 to 6,000 SCCM. In this case, deposition pressure of about 2 to 3 Torr, supply power of about 0.3 to 0.7 KW having a radio frequency of 13.56 MHz and supply power of about 0.4 to 0.8 KW having a low frequency are used. The stress state of the film is controlled to correspond to a compressive stress state of -0.5 to -1.5 dyne/cm^2 by controlling radio frequency power.

When the ratio in flow rate among NH_3, N_2O and N_2 increases, the refractivity of the film increases to about 1.68 or more.

Where a silicon nitride oxide film is used instead of the silicon-rich oxide film 121, the same effect can be obtained.

In this case, the silicon nitride oxide film is deposited to a thickness of about 500 to 3,000 Å. The deposition of the silicon nitride oxide film is carried out under conditions in which the flow rate of SiH_4 is about 200 to 350 SCCM, the flow rate of N_2O is about 1,000 to 4,000 SCCM, the flow rate of NH_3 is about 1,000 to 4,000 SCCM and the flow rate of N_2 is about 3,000 to 6,000 SCCM.

It is preferred that the refractivity of the film be about 1.55 to 1.85 by appropriately controlling the ratio in flow rate of SiH_4 to NH_3. The stress state of the film is controlled to correspond to a compressive stress state of -0.5 to -1.5 dyne/cm^2 by controlling radio frequency power. In this case, deposition pressure of about 2 to 3 Torr, supply power of about 0.4 to 0.6 KW having a radio frequency of 13.56 MHz and supply power of about 0.4 to 0.7 KW having a low frequency are used.

As an example of using the film as a barrier, the film may consist of the silicon-rich oxide film 121 and a silicon nitride oxide film (not shown) formed over the silicon-rich oxide film 121. In this case, the deposition of the films is carried out under the same conditions as that in the case wherein the silicon-rich oxide film 121 and silicon nitride oxide film are selectively used as the barrier.

Thereafter, an SOG film 123 is formed over the silicon-rich oxide film 121 and then baked. The SOG film 123 is used as an interlayer insulating film for providing a planarized surface.

Over the SOG film 123, a second oxide film 125 is then deposited in accordance with the PECVD method. The second oxide film 125 serves as an upper interlayer insulating film.

Then, a second-layer metal wiring 127 is formed on the second oxide film 125. SiN_x is then deposited over the second-layer metal wiring 127, thereby forming a surface protection film 129 which will subsequently be thermally processed.

The silicon nitride film as the surface protection film 129 is deposited to a thickness of about 500 to 1,500Å. The deposition of the silicon nitride film is carried out under the conditions in which the flow rate of SiH_4 is about 450 to 550 SCCM, the flow rate of NH_3 is about 3,000 to 6,000 SCCM and the flow rate of N_2 is about 2,000 to 3,000 SCCM. It is preferred that the refractivity of the

film be about 1.95 to 2.1 by appropriately controlling the ratio in flow rate of SiH_4 to NH_3. In this case, deposition pressure of about 2 to 3 Torr, supply power of about 0.4 to 0.6 KW having a radio frequency of 13.56 MHz and supply power of about 0.4 to 0.7 KW having a low frequency are used. The stress state of the film is controlled to correspond to a compressive stress state of -0.5 to -1.5 dyne/cm^2 by controlling radio frequency power.

Meanwhile, FIG. 3 is a graph depicting the relationship of the refractivity of the insulating film with the insulation-breaking critical voltage between the source n^+ and drain n^+.

As shown in FIG. 3, the insulating-breaking critical voltage between the source and drain increases as the refractivity increases. The refractivity of the silicon-rich oxide film according to the present invention is measured to range from 1.55 to 1.65 whereas the first oxide film formed in accordance with the conventional method exhibits a refractivity of about 1.47. Referring to FIG. 3, it can also be found that the silicon-rich oxide film exhibits stress ranging from -0.5 dyne/cm^2 to -1.5 dyne/cm^2.

In the case of the silicon nitride oxide film, it exhibits a refractivity ranging from 1.68 to 1.8. The silicon nitride oxide film also exhibits stress ranging from -0.5 dyne/cm^2 to -1.5 dyne/cm^2.

On the other hand, FIG. 4 is a graph depicting the relationship between the refractivity of the insulating film and the life of hot carriers in each MOSFET.

Referring to FIG. 4, it can be found that the life of hot carriers is lengthened at a higher refractivity.

As is apparent from the above description, the insulating film

formation method of the present invention provides various effects. That is, it is possible to avoid a field inversion phenomenon from occurring between the drain and source of the parasitic MOSFET as the under interlayer insulating film consists of a silicon-rich oxide film or silicon nitride oxide film. The method of the present invention can also ensure the reliability of hot carriers, thereby achieving an improvement in the operation characteristic of the semiconductor device. In accordance with the method of the present invention, the barrier characteristic of the interlayer insulating film is improved. Accordingly, the method of the present invention can be effectively applied to the fabrication of highly integrated semiconductor devices.

Although the preferred embodiments of the invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.

CLAIMS:

1. A method for forming an interlayer insulating film of a semiconductor device, comprising the steps of:

providing a semiconductor substrate having a under-layer metal wiring formed on an upper surface thereof;

forming a barrier layer on an exposed surface of the semiconductor substrate;

coating a spin-on-glass film over the barrier layer and then baking the spin-on-glass film; and

forming an insulating film over the spin-on-glass film.

2. The method in accordance with claim 1, further comprising the step of sequentially forming a plurality of MOS devices and an insulating film before the formation of the under-layer metal wiring.

3. The method in accordance with claim 1, further comprising the step of forming a silicon oxide film over the exposed surface of the semiconductor substrate before the formation of the barrier layer.

4. The method in accordance with claim 1, wherein the barrier layer is comprised of a silicon-rich oxide film.

5. The method in accordance with claim 4, wherein the silicon-rich oxide film is deposited in accordance with a plasma enhanced chemical vapor deposition method using a reactive gas consisting of SiH_4, N_2O and N_2 under the conditions in which the flow rate of SiH_4 is about 300 to 600 SCCM, the flow rate of N_2O is about 4,000 to 7,000 SCCM and the flow rate of N_2 is about 3,000 to 6,000 SCCM.

6. The method in accordance with claim 4, wherein the silicon-rich oxide film exhibits a refractivity of about 1.55 to 1.65 and has a compressive stress state of -0.5 to -1.5 dyne/cm^2.

7. The method in accordance with claim 1, wherein the barrier layer is comprised of a silicon nitride oxide film.

8. The method in accordance with claim 7, wherein the silicon nitride oxide film is deposited in accordance with a plasma enhanced chemical vapor deposition method using a reactive gas consisting of SiH_4, NH_3, N_2O and N_2 under the conditions in which the flow rate of SiH_4 is about 200 to 350 SCCM, the flow rate of N_2O is about 1,000 to 4,000 SCCM, the flow rate of NH_3 is about 1,000 to 4,000 SCCM and the flow rate of N_2 is about 5,000 to 8,000 SCCM.

9. The method in accordance with claim 7, wherein the silicon nitride oxide film exhibits a refractivity of about 1.55 to 1.85 and has a compressive stress state of -0.5 to -1.5 dyne/cm^2.

10. The method in accordance with claim 1, wherein the barrier layer has a thickness of about 500 to 3,000Å.

11. The method in accordance with claim 1, wherein the insulating film is comprised of a silicon oxide film.

12. The method in accordance with claim 1, further comprising the steps of forming an upper-layer metal wiring on the insulating film, and forming a protective film over the entire exposed surface of the resulting structure obtained after the formation of the upper-layer metal wiring.

13. A method for forming an interlayer insulating film of a semiconductor device, comprising the steps of:

providing a semiconductor substrate having a under-layer metal wiring formed on an upper surface thereof;

forming a silicon-rich oxide film over an exposed surface of the semiconductor substrate, and forming a silicon nitride oxide film over the silicon-rich oxide film;

forming a spin-on-glass film over the silicon nitride oxide

film; and

forming an oxide film over the spin-on-glass film.

14. The method in accordance with claim 13, wherein the silicon-rich oxide film is deposited in accordance with a plasma enhanced chemical vapor deposition method using a reactive gas consisting of SiH_4, N_2O and N_2 under the conditions in which the flow rate of SiH_4 is about 300 to 600 SCCM, the flow rate of N_2O is about 4,000 to 7,000 SCCM and the flow rate of N_2 is about 3,000 to 6,000 SCCM.

15. The method in accordance with claim 13, wherein the silicon-rich oxide film exhibits a refractivity of about 1.55 to 1.65 and has a compressive stress state of -0.5 to -1.5 dyne/cm^2.

16. The method in accordance with claim 13, wherein the silicon nitride oxide film is deposited in accordance with a plasma enhanced chemical vapor deposition method using a reactive gas consisting of SiH_4, NH_3, N_2O and N_2 under the conditions in which the flow rate of SiH_4 is about 200 to 350 SCCM, the flow rate of N_2O is about 1,000 to 4,000 SCCM, the flow rate of NH_3 is about 1,000 to 4,000 SCCM and the flow rate of N_2 is about 5,000 to 8,000 SCCM.

17. The method in accordance with claim 13, wherein the silicon nitride oxide film exhibits a refractivity of about 1.55 to 1.85 and has a compressive stress state of -0.5 to -1.5 dyne/cm^2.

18. The method in accordance with claim 13, further comprising the steps of forming an upper-layer metal wiring on the silicon nitride oxide film, and forming a protective film over the entire exposed surface of the resulting structure obtained after the formation of the upper-layer metal wiring.

19. The method in accordance with claim 13, further comprising the step of sequentially forming a plurality of MOS devices and an insulating film before the formation of the under-layer metal

wiring.

20. The method in accordance with claim 13, wherein the protective film exhibits a refractivity of about 1.95 to 2.1 and has a compressive stress state of -0.5 to -1.5 dyne/cm^2.

21. A method for forming an interlayer insulating film of a semiconductor device substantially as hereinbefore described with respect to any one of Figures 2 to 4.

The Patent Office

Application No:	GB 9619116.8	**Examiner:**	Robin Hradsky
Claims searched:	1-21	**Date of search:**	25 November 1996

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H1K (KJAB, KJAP, KJACX, KJAX, KHAE)

Int Cl (Ed.6): H01L 21/314, 21/316

Other: Online:WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
Y	EP0249173 A1	Rockwell (Fig 4)	1,13
Y	US5003062 A	TSM (Fig 3 and col 5 line 43 to col 6 line 50)	1,13

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.